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(71) Applicant (for all designated States except US): TELEFON-AKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S-126 25 Stockholm (SE).

(72) Inventor; and

(75) Inventor/Applicant (for US only): NORSTRÖM, Hans [SE/SE]; Mårdstigen 3, S-171 93 Solna (SE).

(74) Agents: BOHLIN, Björn et al.; Telefonaktiebolaget LM Ericsson, Patent and Trademark Dept., S-126 25 Stockholm (SE).

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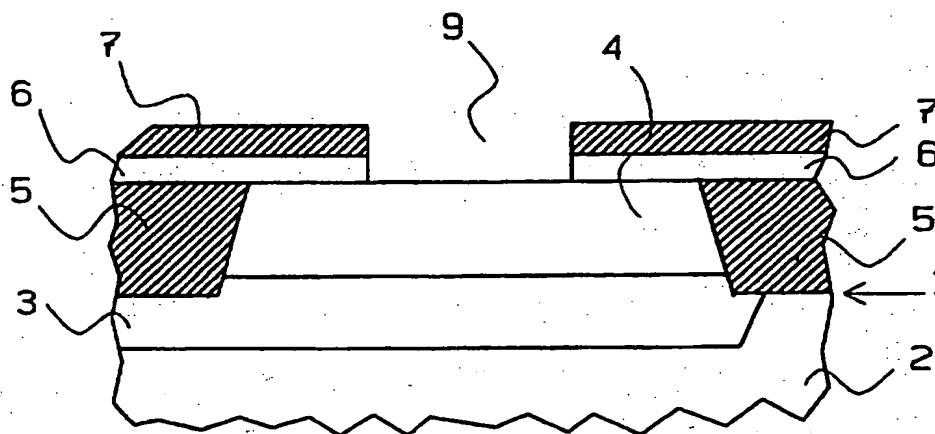
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## (57) Abstract

In a method of selectively etching in the fabrication of a semiconductor device, an amorphous layer (6) of said semiconductor material is deposited on a crystalline substrate (1) of the same semiconductor material. At least one dielectric layer (7) is deposited on the amorphous layer (6) such as to prevent crystallization of the amorphous layer (6). The dielectric layer (7) is preferably deposited with the aid of either a PECVD, SACVD, MBE technique or a spin-on technique. The resultant structure (1) is patterned and the dielectric layer (7) and the amorphous semiconductor layer (6) then etched away within a predetermined region (9). The method may form a sub-stage in the manufacture of a bipolar transistor having a self-registered base-emitter structure.

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## METHOD IN THE MANUFACTURING OF A SEMICONDUCTOR DEVICE

## FIELD OF INVENTION

The present invention relates to a method of etching  
5 selectively when manufacturing semiconductor devices and to a  
method of manufacturing bipolar transistors while applying the  
selective etching method.

## DESCRIPTION OF THE PRIOR ART

10

The trend in the design and manufacture of integrated circuits  
leans towards progressively smaller individual components of  
progressively higher performances. For instance, the dimensions  
of bipolar transistors are becoming progressively smaller, both  
15 horizontally and vertically, so as to increase packing  
densities and transistor speeds. Manufacturing precision has  
therewith become progressively more important, both with regard  
to individual process stages and with regard to the alignment  
between different layers.

20

There is normally used at present in the manufacture of bipolar  
high frequency transistors a technique that employs a self-  
registered base-emitter structure (T. H. Ning et al, "Self-  
Aligned npn Bipolar Transistors", IEDM Techn. Dig., pages 823-  
25 824, 1980), which enables the transistor cell to be made  
smaller while obtaining a reduced base-collector capacitance  
and a reduced base resistance when the extrinsic base is  
connected to the intrinsic base in the immediate proximity of  
the emitter. Several variants of this method are known to the  
30 art.

- U.S. Patent 5,266,504 describes a method of manufacturing a self-registered bipolar transistor in which the base is grown epitaxially and the emitter is formed by the deposition of an amorphous silicon layer followed by a polycrystalline silicon layer, whereafter the structure is patterned and etched. The amorphous silicon layer is then recrystallized by SPE (Solid Phase Epitaxy). This method is able to provide a thin base and a sharp and well-controlled emitter-base junction.
- U.S. 4,988,632 teaches the deposition of a polycrystalline silicon layer or an amorphous silicon layer on a substrate and doping of the layer. A layer of LTO (Low Temperature Oxide) or some other dielectric is deposited on said silicon layer, whereafter the structure is patterned and etched to provide a base electrode and emitter opening. U.S. 5,213,989 teaches a method of depositing a polycrystalline silicon layer, an amorphous silicon layer or some similar silicon-based layer on a substrate and doping said layer, whereafter a dielectric layer, preferably a TEOS-based (Tetra Ethyl Ortho Silicate-based) oxide is deposited over the silicon layer. The structure is patterned and etched in a known manner. It is not evident from U.S. 4,988,632 and U.S. 5,213,989 that the silicon layers shall be amorphous when etching out the emitter openings.
- Those problems that occur when selectively etching away a polycrystalline silicon layer from a silicon substrate involve difficulties in stopping the etching process so that the polycrystalline silicon layer is removed completely without penetrating the substrate too deeply. The polycrystalline silicon layer is also etched at different speeds along different crystal directions and at grain boundaries, resulting in etching residues, so-called pillars, or in irregularities in

the etched surface, so-called facets, and in blunt or dull edges in the etched openings. When the polycrystalline layer is to be doped by ion implantation, there is a risk of channelization of the dopant in grain boundaries or along  
5 crystal directions, meaning that the degree of doping cannot be controlled. Particularly when etching out the emitter opening in the manufacture of bipolar transistors that have a self-registered base-emitter structure, it is of the greatest importance that the aforesaid problems are overcome, since when  
10 the substrate is etched too deeply there is a risk of obtaining an excessively high series resistance or no electrical contact at all between intrinsic and extrinsic base. When doping to achieve a given type of doping, n or p, to form the emitter, there is also the risk of forming so-called pipes, i.e.  
15 channels of said doping type transversely through the intrinsic base, resulting in emitter leakage. These pipes are formed generally as a result of etching residues, so-called pillars.

#### SUMMARY OF THE INVENTION

20

The object of the present invention is to resolve the aforesaid problems and thus produce semiconductor components, particularly bipolar transistors, of higher quality and/or higher performance and/or of smaller size than those  
25 semiconductor components produced by hitherto known methods.

To this end, the inventive method includes the etching of amorphous silicon. Such silicon lacks crystal structures. The use of amorphous silicon thus removes many of the problems and  
30 drawbacks encountered when etching polycrystalline silicon.

The inventive method involves depositing an amorphous silicon layer on a crystalline silicon substrate. According to the invention, there is deposited on the amorphous silicon layer a protective dielectric layer such as to prevent crystallization of the amorphous layer. The dielectric layer is preferably deposited by one of the following methods: PECVD (Plasma Enhanced Chemical Vapor Deposition), SACVD (Sub Atmospheric Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy) or with the aid of a spin-on technique. The dielectric layer is preferably comprised of PETEOS (Plasma Enhanced Tetra Ethyl Ortho Silicate). The resultant structure is patterned, whereafter the dielectric layer and the amorphous silicon layer are etched, for instance dry-etched, within a predetermined area.

The inventive etching method provides structures which have sharply defined edges and smooth pronounced etched surfaces in the absence of pillar or facet formation tendencies. Good etching selectivity between amorphous and crystalline silicon is also obtained. This results in semiconductor components of improved performance in relation to earlier semiconductor components. Particularly when fabricating a bipolar transistor having a self-registered base-emitter structure, the aforesaid etching process can be applied when etching-away the emitter opening in a manner which enables semiconductor devices of very small dimensions (length scales in the sub-micrometer range) to be produced. The advantages afforded by the present method include good etching selectivity when etching amorphous silicon on crystalline silicon, good CD control (Critical Dimension control), i.e. good control of the dimensions of the etched opening, and the avoidance of the risk of channelization of the dopant in the case of ion implantation processes.



## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in more detail with  
5 reference to the accompanying drawings, in which Figs. 1-2 are  
cross-sectional views which illustrate two inventive method  
steps when etching a silicon layer on a silicon surface, and  
Figs. 3-6 are cross-sectional views illustrating four inventive  
method steps in the fabrication of a bipolar transistor having  
10 a self-registered base-emitter structure departing from the  
structure illustrated in Fig. 2.

## DESCRIPTION OF PREFERRED EMBODIMENTS

15 Shown in Fig. 1 is a silicon substrate 1, wherein the silicon  
may be a monocrystalline, a polycrystalline or a  
microcrystalline silicon, but which is preferably a  
monocrystalline silicon. As in the Fig. 1 illustration, the  
substrate 1 may have various defined active regions 2-5, which  
20 will be described below in more detail, although the substrate  
may also be homogenous. Any surface oxide present on the  
substrate 1, said surface oxide possibly having a thickness of  
some tens of Ångströms, can be removed by conveniently dipping  
the substrate in an HF bath or in HF vapour. In accordance with  
25 the invention, there is deposited on the substrate 1 a layer 6  
of amorphous silicon, so-called  $\alpha$ -Si to a thickness of some  
hundred nanometers, preferably with the aid of CVD technique  
(Chemical Vapor Deposition) at 550-560°C. The amorphous silicon  
may alternatively be deposited at another temperature and/or  
30 with the aid of some other technique, such as PECVD or  
sputtering. In accordance with the invention, there is

deposited on the amorphous silicon layer 6 a protective dielectric layer 7 such as to prevent crystallization of the amorphous layer 6. This is ensured when the dielectric layer 7 is deposited at a temperature below about 500°C and over a relatively short period of time. The so-called single wafer technique is preferably used in this regard, i.e. a technique in which one wafer is processed at a time, which gives shorter deposition times. Examples of such techniques are PECVD, SACVD, MBE and the spin-on technique. The dielectric layer 7 may be comprised of a nitride or an oxide for instance, although it will preferably comprise a silicate. The silicate used will conveniently be PETEOS, i.e. TEOS (Tetra Ethyl Ortho Silicate), which is deposited with PECVD. This results in a high quality layer of low particle density and porosity, and also affords good control over layer thickness. The layer 7 shall be deposited to a thickness in the order of some hundred nanometers. A preferred deposition temperature is between 250 and 400°C. Although not shown, one or more additional dielectric layers may be deposited on the structure.

The structure, referenced 8 in Fig. 1, is then patterned with the aid of a conventional photolithographic process, whereafter the mutually superimposed additional dielectric layer (not shown) when present, the dielectric layer 7 and the amorphous silicon layer 6 are removed within a predetermined region or area 9 in an etching step. The upper side of the substrate 1 is thus exposed within the region 9. The dielectric layer 7 may be etched with the aid of an anisotropic dry etching process, for instance with the aid of  $\text{CHF}_3/\text{O}_2$  plasma or  $\text{C}_2\text{F}_6$  plasma.

According to the present invention, the amorphous silicon layer 6 is preferably etched in a dry etching process, which may be anisotropic, e.g. an HBr and/or  $\text{Cl}_2$  plasma.

The amorphous silicon, which lacks macroscopic crystal structures, is rich in defects and therefore has greater free energy than polycrystalline and monocrystalline silicon. It is therefore possible to achieve etching selectivity between

5 amorphous silicon and polycrystalline or monocrystalline silicon. The greatest selectivity is obtained with monocrystalline silicon. In this case, it is possible to over-etch such as to positively etch away all amorphous silicon without penetrating the substrate too deeply. When etching

10 amorphous silicon, no undesirable etching is obtained along grain boundaries or crystal surfaces, therewith resulting in smooth etched surfaces. When over-etching into the underlying monocrystalline silicon, a smooth surface is obtained in the absence of replica or facets of the grain structure, so-called

15 reproduction of facet crystal grains or residual crystal grains, so-called pillars, as would possibly be the case when etching polycrystalline or microcrystalline silicon. Furthermore, an opening that is etched out in amorphous silicon will have sharper edges and smoother side walls than a

20 corresponding opening that is etched-out in polycrystalline silicon. It is highly important to achieve good CD control, i.e. control over the dimensions of the etched opening, particularly when fabricating semiconductor devices within the sub- $\mu\text{m}$  range, such control being achieved when etching in

25 amorphous silicon.

The amorphous silicon layer 6 may optionally be doped prior to depositing the protective dielectric layer 7, said doping conveniently being effected by ion implantation. Ion

30 implantation in amorphous silicon avoids channelization of the dopant in grain boundaries and crystal directions, such channelization normally occurring when ion implanting in

crystalline silicon. When the layer 6 is doped p+, there is used the gas  $\text{BF}_3$ , which is ionized and accelerated, wherein desired ions are sorted out and allowed to penetrate into the silicon. The gas used is preferably  $\text{BF}_2^+$  because this ion is  
5 produced in large quantities in the ionization process and boron will diffuse to a shallower depth in the substrate in a possible later heat-treatment process. Incorporation of fluorine in the amorphous silicon layer 6 can also contribute towards enabling the natural oxide boundary layer between the  
10 amorphous silicon layer 6 and the underlying substrate 1 to be broken-up more easily in a possible later heat-treatment process.

One of the aforescribed methods can be used conveniently in  
15 the fabrication of diodes, metal semiconductor devices, transistors or other types of semiconductor components which include at least one etching step of silicon on silicon.

According to the present invention, the aforescribed method  
20 steps are used as a sub-process in the fabrication of an npn-type bipolar transistor having a self-registered base-emitter structure, for instance.

The method of fabricating a bipolar transistor departs from the  
25 structure illustrated in Fig. 2 having defined active regions 2, i.e. as seen from the bottom a p-doped region 2, an  $\text{n}^+$ -doped layer 3 for a collector electrode, and nearest the surface an n-doped layer 4, which is surrounded by an electrically insulating region 5.

30 The window 9 shown in Fig. 2 will form an emitter opening, whereas the amorphous silicon layer 6 will form an extrinsic

base.

As shown in Fig. 3, there is then grown on the structure shown in Fig. 2 a thin thermal oxide layer 10 having a thickness of one or more tens of nanometers (Fig. 3) at a temperature which causes the amorphous silicon layer 6 to crystallize. This now crystalline silicon layer is referenced 6' in Fig. 3. A suitable temperature range in this regard is 700-1150°C. Parallel herewith, the dopants are driven into the substrate 1 from the doped, crystalline silicon layer 6' to form a doped area or region 11. A p-doped, intrinsic base 12 is formed by ion implantation of, e.g.,  $\text{BF}_3^+$  in the substrate 1 through the medium of the thin oxide layer 10. The p<sup>+</sup>-region 11 enables electric contact to be obtained between the intrinsic base 12 and the extrinsic base 6'.

A layer 13 of electrically insulating material is then deposited conformly over the structure according to Fig. 3. The layer 13 will preferably have a thickness of some hundred nanometers and will preferably consist of a nitride, for instance silicon nitride  $\text{Si}_3\text{N}_4$ , and be deposited with the aid of LPCVD technique (Low Pressure Chemical Vapor Deposition). The resultant structure is shown in Fig. 4.

The nitride layer 13 is re-etched anisotropically in a plasma etching process until a thin oxide layer (not shown) remains on top of the substrate 1 in the emitter opening 9. A nitride string or so-called nitride spacer 13' remains along the side walls of the emitter opening 9. This oxide layer (not shown) is then removed by a selective plasma etching process or a wet etching process, therewith exposing the substrate surface 14 in the emitter opening 9. The resultant structure is shown in Fig.

5. This structure is then dipped, optionally in an HF bath or in HF vapour, to remove surface oxide, whereafter an emitter layer (not shown) of polycrystalline or amorphous silicon is deposited on the structure shown in Fig. 5. The emitter layer is deposited preferably to a thickness of some hundred nanometers and is  $n^+$ -doped by implanting arsenic, for instance. The structure is then heat-treated, wherein the dopant (arsenic) is driven into the substrate 1 and forms an  $n^+$ -doped region 16. During the heat-treatment process, boron diffuses down in the substrate, wherewith the intrinsic base and the  $p^+$ -doped region become deeper, as evident from the regions referenced 12' and 11' respectively in Fig. 6. A very shallow emitter ( $n^+$ )-base(p)-junction can be obtained by carrying out the method steps with precision and by carefully controlling the steps. The emitter layer (not shown) is patterned lithographically and plasma etched in a conventional manner to define an emitter 15 in the emitter opening 9, as shown in Fig. 6.
- Alternatively, the emitter 15 can be grown epitaxially and doped at the same time as it is grown. No patterning or etching of the emitter is necessary when using selective epitaxy. The spacer 13' isolates the extrinsic base 6' electrically from the emitter 15 in both of these cases.
- A further oxide layer is then optionally deposited on the structure shown in Fig. 6, whereafter the structure is patterned and etched to form contact holes.
- It will be understood that the aforescribed method can also be used in the fabrication of pnp-transistors, after changing the dopants. In this regard, the amorphous silicon layer 6 and

the intrinsic base 12 are preferably doped with  $\text{PH}_3$  or  $\text{AsH}_3$ , whereas the collector 3, 4 and the emitter 15, 16 are doped with  $\text{BF}_3$ .

- 5 The advantages that are afforded by a method of the  
aforedescribed kind include greater precision in manufacture,  
the possibility of reducing dimensions, meaning lower base-  
collector capacitance and lower base resistance of the  
transistor, and the avoidance of the risk of poor or no  
10 electrical contact between intrinsic and extrinsic bases, by  
virtue of the fact that it is unnecessary to etch out the  
emitter opening with a powerful over-etching procedure.

- It will be understood that the aforedescribed embodiments of  
15 the inventive method can also be implemented with other  
semiconductor materials than silicon. For instance, an  
amorphous germanium layer can be etched from a crystalline  
layer of the same material, i.e. germanium, while retaining the  
aforedescribed advantages.

## CLAIMS

1. A method etching selectively in the fabrication of a semiconductor device, characterized by
  - depositing an amorphous layer (6) of semiconductor material on a crystalline substrate (1) of the same semiconductor material;
  - depositing at least one dielectric layer (7) on the amorphous layer (6) such as to prevent crystallization of said amorphous layer (6); and
  - patterning the resultant structure (8) and thereafter etching away the dielectric layer (7) and the amorphous semiconductor layer (6) within a predetermined area or region (9).
2. A method according to Claim 1, characterized by depositing the dielectric layer (7) with the aid of either a PECVD, SACVD, MBE technique or a spin-on technique.
3. A method according to Claim 1, characterized by forming the dielectric layer (7) from PETEOS.
4. A method according to any one of Claims 1-3, characterized by depositing the amorphous layer (6) on the substrate (1) with the aid of a CVD technique.
5. A method according to any one of Claims 1-4, characterized by depositing the dielectric layer (7) at a temperature of between 250 and 400°C.
6. A method according to any one of Claims 1-5, characterized by using silicon as the semiconductor material.



7. A method relating to the manufacture of a bipolar transistor having a self-registered base-emitter structure, characterized by

- 5 - depositing a layer (6) of amorphous silicon on a substrate (1) of crystalline silicon having an upper region (3-4) of a first conductor type;
  - doping the amorphous silicon layer (6) with a dopant to form a second conductor type;
- 10 - depositing at least one dielectric layer (7) on the amorphous silicon layer (6) in a manner such as to prevent crystallization of the amorphous silicon layer (6);
  - patterning the resultant structure (8) and thereafter etching away the dielectric layer (7) and the amorphous silicon layer (6) within a predetermined region such as to define an emitter opening (9);
- 15 - growing a thermal oxide (10) on the resultant structure, wherein the amorphous silicon layer (6) is converted to a polycrystalline silicon layer (6');
  - 20 - forming an intrinsic base (12) of the same conductor type as said polycrystalline layer (6') by doping through the thermal oxide (10);
  - depositing a layer (13) of electrically insulating material on the resultant structure and thereafter etching the structure anisotropically until a thin oxide layer remains on the substrate in the emitter opening (9) and in such a manner that a spacer (13') of said electrically insulating material remains along the side walls of the emitter opening (9);
- 25

- removing said thin oxide layer;
  - forming an emitter contact (15) in the emitter opening (9) and doping said emitter contact to said first conductor type; and
- 5    - heat-treating the structure to form an emitter-base junction (16, 12') in the substrate by out diffusion of the dopants from the emitter contact (15).
8.    A method according to Claim 7, characterized by depositing
- 10    the dielectric layer (7) with the aid of either a PECVD, SACVD, MBE technique or a spin-on technique.
9.    A method according to Claim 6, characterized by using
- 15    PETEOS as the dielectric layer (7).
10.    A method according to any one of Claims 7-9, characterized by forming the emitter contact (15) by depositing a layer of polycrystalline silicon and doping said layer to said first conductor type, and thereafter patterning the doped layer
- 20    lithographically and plasma-etching said layer.
11.    A method according to any one of Claims 7-10, characterized by doping the amorphous silicon layer (6) by  $\text{BF}_3$  ion implantation.
- 25    12.    A method according to any one of Claims 7-11, characterized by depositing the dielectric layer (7) at a temperature of between 250 and 400°C.
- 30    13.    A method according to any one of Claims 7-12, characterized by forming the spacer (13') from an electrically

insulating nitride material (13) and depositing said layer to a thickness of some hundred nanometers with the aid of an LPCVD technique.

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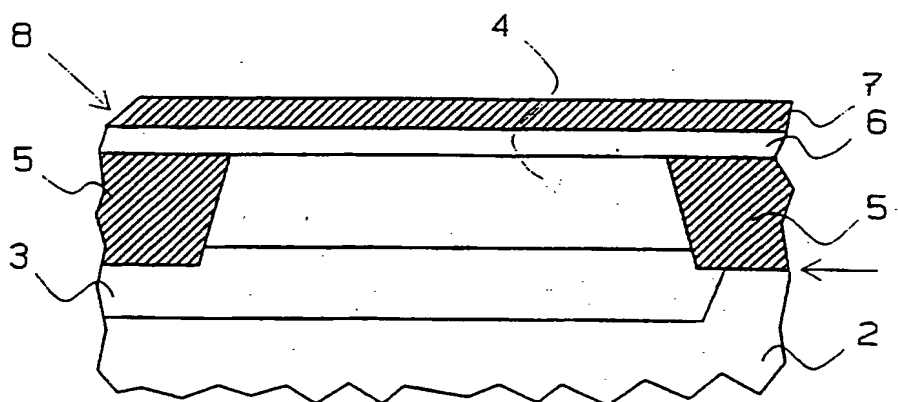


Fig. 1

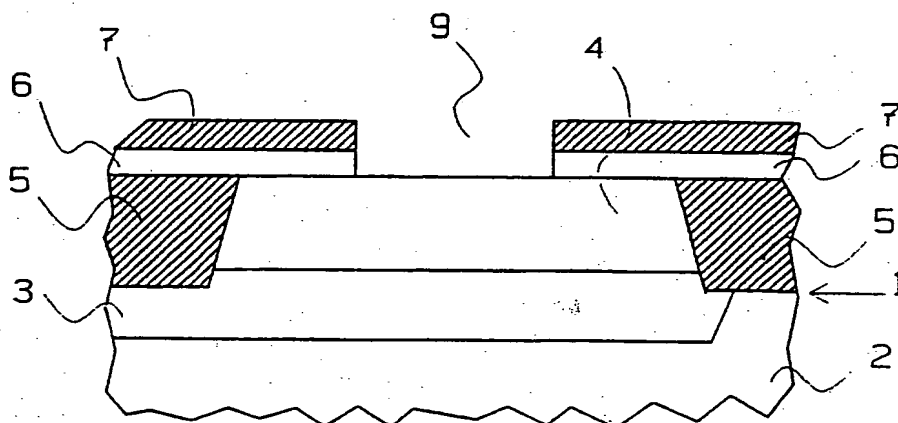


Fig. 2

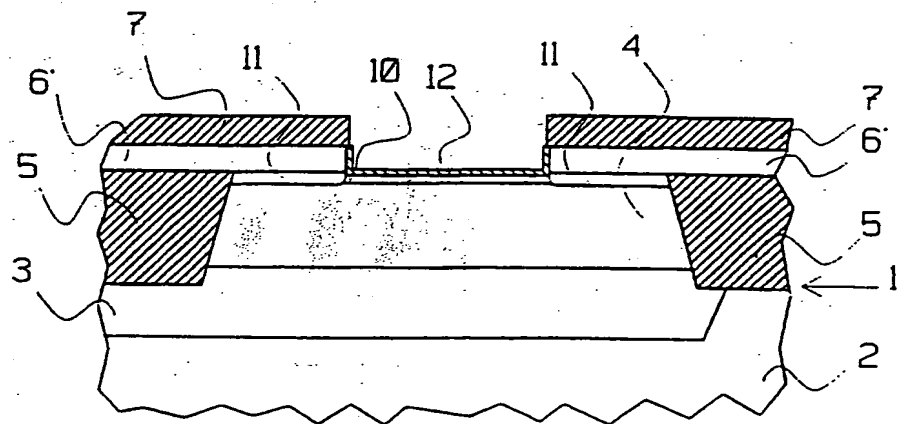


Fig. 3

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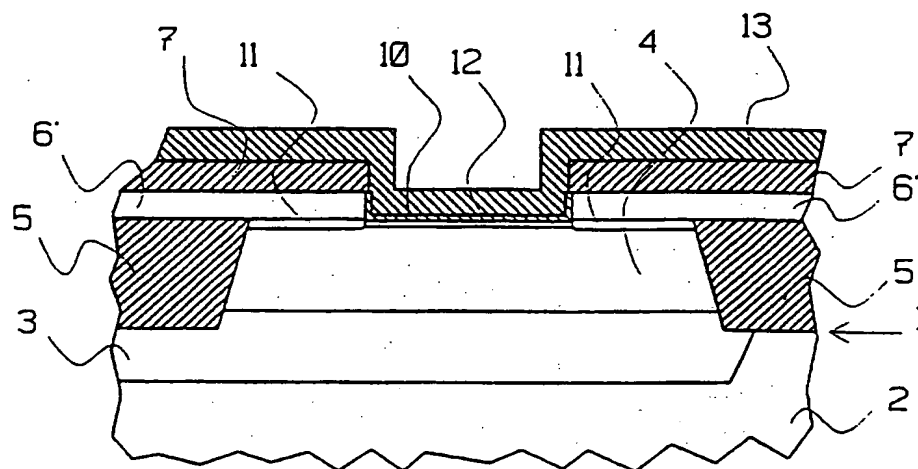


Fig. 4

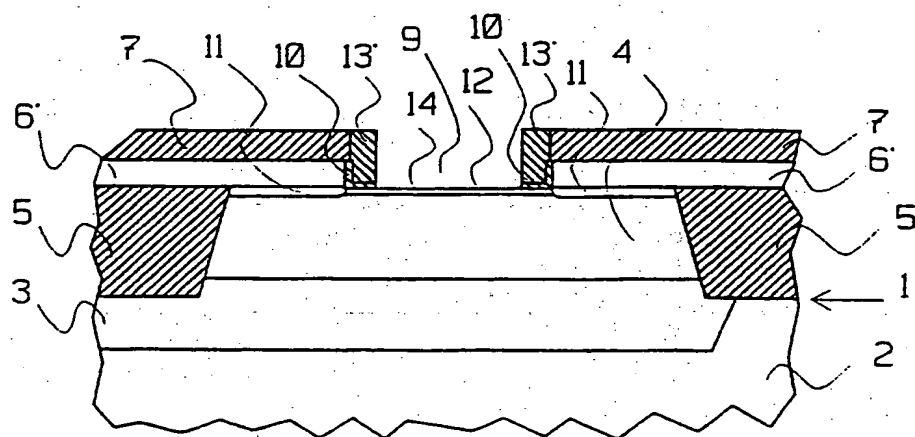


Fig. 5

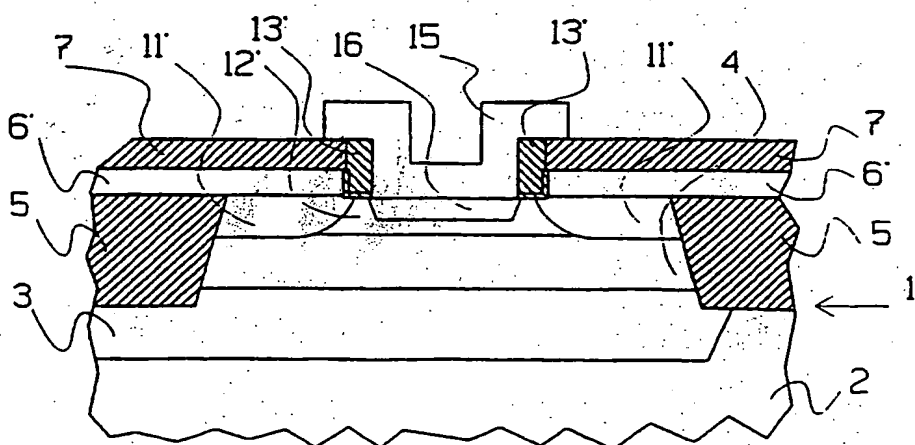


Fig. 6

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 96/01511

## A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 21/316, H01L 21/322, H01L 21/328

According to International Patent Classification (IPC) or to both national classification and IPC

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Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 2, 350, 351, 434

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4792501 A (D.D. ALLRED ET AL), 20 December 1988 (20.12.88), column 2, line 54 - column 3, line 44; column 4, line 13 - column 6, line 19, figures 1a, b	1-6
A	---	7-9
Y	Appl. Phys. Lett, Volume 58, No 15, April 1991, S.J. Jeng et al, "Structure, properties, and thermal stability of in situ phosphorus-doped hydrogenated microcrystalline silicon prepared by plasma-enhanced chemical vapor deposition" page 1632 - page 1634	1-6
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☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Facsimile No. +46 8 666 02 86

Authorized officer

Pär Moritz

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PCT/SE 96/01511

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5213989 A (FITCH ET AL), 25 May 1993 (25.05.93), column 2, line 54 - column 4, line 28, figures 1-3	1-6
A	--	7-13
Y	EP 573823 A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO), 15 December 1993 (15.12.93)	1-6
A	--	7-9
Y	US 4960719 A (S. TANAKA ET AL), 2 October 1990 (02.10.90), column 2, line 54 - column 3, line 44; column 4, line 13 - column 6, line 19, figures 1a-c, claim 1	1-6
A	--	7-9
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